We claim:

1. A pixel element for sensing light impinging on the pixel element and providing a non-destructive readout representative of the amount of impinging light, comprising:

a substrate capable of forming localized depletion regions in the presence of an applied voltage at the regions;

an insulating layer formed on said substrate;

a collection capacitor electrode in contact with said insulating layer and being electrically isolated from said substrate by said insulating layer, wherein said insulating layer and collection capacitor electrode are transparent to light;

a transfer electrode located adjacent said collection capacitor electrode and being electrically isolated from said substrate by said insulating layer;

a readout capacitor electrode located adjacent said transfer electrode and in contact with said insulating layer, said readout capacitor electrode being spaced from said collection capacitor electrode and being electrically isolated from said substrate by said insulating layer; and

a readout transistor having an insulated gate connected to said readout capacitor electrode, with said transistor providing an output signal that is indicative of the quantity of charge stored in said substrate under said readout capacitor electrode, whereby said readout transistor provides a non-destructive readout of the stored charge.

2. A pixel element as defined in claim 1, further comprising:

a dump electrode adjacent one of said capacitor electrodes; and

a supply connecting region in said substrate located adjacent said dump electrode and spaced from said one capacitor electrode, wherein, when a bias voltage is applied to said dump electrode and said supply connecting region of said substrate is connected to a supply voltage, charge stored in said substrate underneath said readout capacitor electrode is transferred to said supply connecting region to thereby reset said pixel element.

3. A pixel element as defined in claim 1, further comprising an output transistor having an input connected to said output of said readout transistor, a gate connected to receive a pixel select signal, and an output, with said output transistor being operable to provide said output signal to its output in response to receiving the pixel select signal on its gate.

4. A pixel element as defined in claim 1, wherein said collection capacitor electrode is located within said insulating layer in spaced relation to said substrate.

5. A pixel element as defined in claim 1, wherein said pixel element comprises a metal oxide semiconductor structure.

6. A pixel element as defined in claim 1, wherein said pixel element comprises a polycrystalline silicon - oxide - semiconductor structure.

7. A pixel element as defined in claim 1, wherein said insulating layer comprises silicon dioxide.

8. A pixel element as defined in claim 1, wherein said collection capacitor electrode comprises polycrystalline silicon.

9. A pixel element as defined in claim 1, wherein said substrate comprises crystalline silicon.

10. A pixel element as defined in claim 1, wherein said readout capacitor electrode is spaced from said collection capacitor electrode such that, when a bias voltage is applied to said capacitor electrodes, a depletion region is formed in said substrate below each of said capacitor electrodes with said depletion regions being electrically isolated from each other and, when a bias voltage is applied to said transfer electrode, a depletion region is formed in said substrate that joins the depletion regions located below said capacitor electrodes.

11. A pixel element as defined in claim 1, further comprising a biasing transistor having a supply input connected to receive a bias voltage, an output

connected to said readout capacitor electrode, and a gate connected to receive a bias control signal, wherein, when said biasing transistor is actuated, the biasing voltage is applied to said readout capacitor electrode to thereby form a depletion region in said substrate underneath said readout capacitor electrode and, when said biasing transistor is not actuated, said readout capacitor electrode is isolated from the biasing voltage to thereby enable readout of data from said readout capacitor electrode using said readout transistor.

12. A pixel element as defined in claim 1, wherein said transfer electrode overlies at least a portion of said readout capacitor electrode.

13. An image sensor comprising an array of pixel elements constructed according to claim 1.

14. An image sensor as defined in claim 13, further comprising a control circuit connected to said array of pixel elements, said control circuit being operable to select individual pixel elements within said array and access the output of said readout transistor from a selected pixel element.

15. An image sensor as defined in claim 14, wherein said control circuit includes a plurality of electrical connections to said pixel elements to selectively provide voltages on said electrodes, with said control circuit being operable to provide a voltage on any of said electrodes that creates a depletion region in said substrate below that electrode, and wherein said control circuit is further operable to apply a voltage to said collection capacitor electrode during an integration period to thereby collect charge in the depletion region below said collection capacitor electrode, and then to apply a voltage to said transfer electrode and said readout capacitor electrode to thereby transfer collected charge from the depletion region below said collection capacitor electrode to the depletion region below said readout depletion region, and to thereafter remove the applied voltage from said collection capacitor electrode to thereby collapse the depletion region below said collection capacitor electrode and allow charge underneath said collection capacitor electrode to migrate to the depletion region below said readout capacitor electrode, whereby the depletion region below

said readout capacitor electrode contains a charge indicative of the amount of light that impinged upon said collection capacitor electrode during the integration period.

16. A pixel element for sensing light impinging on the pixel element and providing a non-destructive readout representative of the amount of impinging light, comprising:

a silicon-based substrate capable of forming localized depletion regions in the presence of an applied voltage at the regions;

a transparent insulating layer formed on said substrate;

a first polycrystalline silicon electrode formed as a collection electrode that is transparent to light and that is located within said insulating layer such that it is electrically isolated from said substrate by said insulating layer, said collection electrode being spaced from said substrate such that a first depletion region can be formed in said substrate in response to a bias voltage being applied to said collection electrode, wherein light impinging upon said pixel element at said collection electrode is transmitted through said insulating layer and collection electrode and into said substrate where the impinging light forms electron-hole pairs with the electrons being collected in the substrate near the collection electrode;

a second polycrystalline silicon electrode formed as a transfer electrode located laterally adjacent said collection electrode, said transfer electrode being spaced from said substrate by said insulating layer such that a second depletion region can be formed in said substrate in response to a bias voltage being applied to said transfer electrode;

a third polycrystalline silicon electrode formed as a readout electrode that is located within said insulating layer such that it is electrically isolated by said insulating layer from said substrate and said collection and transfer electrodes, said readout electrode being spaced from said substrate such that it provides a readout of charge stored in said substrate under said readout electrode, wherein said second depletion region under said transfer electrode overlaps said first depletion region and permits charged stored in said first depletion region to be transferred to a location in said substrate underneath said readout electrode;

a readout transistor having an insulated gate connected to said readout electrode, with said transistor providing an output signal that is indicative of the

quantity of charge stored in said substrate under said readout electrode, whereby said readout transistor provides a non-destructive readout of the stored charge;

an output transistor having an input connected to said output of said readout transistor, a gate connected to receive a pixel select signal, and an output, with said output transistor being operable to provide said output signal to its output in response to receiving the pixel select signal on its gate;

a dump electrode adjacent one of said first, second, and third electrodes; and

a supply connecting region in said substrate located adjacent said dump electrode and spaced from said one electrode, wherein, when a bias voltage is applied to said dump electrode with said supply connecting region being connected to a supply voltage, charge stored in said substrate underneath said readout electrode is transferred to said supply connecting region to thereby reset said pixel element.

17. A pixel element as defined in claim 16, further comprising a biasing transistor having a supply input connected to receive a bias voltage, an output connected to said readout electrode, and a gate connected to receive a bias control signal, wherein, when said biasing transistor is actuated, the biasing voltage is applied to said readout electrode to thereby form a third depletion region in said substrate underneath said readout electrode with said first and third depletion regions being separated by an intervening space and said second depletion region being located within said intervening space and overlapping both said first and third depletion regions, and wherein, when said biasing transistor is not actuated, said readout electrode is isolated from the biasing voltage to thereby enable readout of data from said readout electrode using said readout transistor.

18. A pixel element as defined in claim 16, wherein said transfer electrode overlies said readout electrode and said second depletion region is located underneath said readout electrode.

19. A memory element for storing data and providing a non-destructive analog readout of the data, comprising:

a substrate capable of forming localized depletion regions in the presence of an applied voltage at the regions;

an insulating layer formed on said substrate;

a collection capacitor electrode in contact with said insulating layer and being electrically isolated from said substrate by said insulating layer, said collection capacitor electrode being spaced from said substrate such that a first depletion region can be formed in said substrate in response to a bias voltage being applied to said collection capacitor electrode, whereby said substrate can store charge supplied to or generated in said first depletion region;

a transfer electrode located adjacent said collection capacitor electrode and being spaced from said substrate such that a second depletion region can be formed in said substrate in response to a bias voltage being applied to said transfer electrode;

a readout capacitor electrode located adjacent said transfer electrode and in contact with said insulating layer, said readout capacitor electrode being spaced from said substrate such that it provides a readout of charge stored in said substrate under said readout capacitor electrode, wherein said second depletion region under said transfer electrode overlaps said first depletion region and permits charged stored in said first depletion region to be transferred to a location in said substrate underneath said readout capacitor electrode;

a readout transistor having an insulated gate connected to said readout capacitor electrode, with said transistor providing an output signal that is indicative of the quantity of charge stored in said substrate under said readout capacitor electrode, whereby data can be temporarily stored in said first depletion region as stored charge which can then be transferred using said second depletion region to a location underneath said readout capacitor electrode and then used by said readout transistor to provide a non-destructive analog readout of the data.

20. A memory element as defined in claim 19, further comprising:

a dump electrode adjacent one of said capacitor electrodes; and

a supply connecting region in said substrate located adjacent said dump electrode and spaced from said one capacitor electrode, wherein, when a bias voltage is applied to said dump electrode and said supply connecting region of said substrate is connected to a supply voltage, charge stored in said substrate underneath said readout capacitor electrode is transferred to said supply connecting region to thereby reset said memory element.

21. A memory element as defined in claim 19, further comprising an output transistor having an input connected to said output of said readout transistor, a gate connected to receive a memory element select signal, and an output, with said output transistor being operable to provide said output signal to its output in response to receiving the memory element select signal on its gate.

22. A memory element as defined in claim 19, wherein said collection capacitor electrode is located within said insulating layer in spaced relation to said substrate.

23. A memory element as defined in claim 19, wherein said memory element comprises a metal oxide semiconductor structure.

24. A memory element as defined in claim 19, wherein said memory element comprises a two layer polycrystalline silicon - oxide semiconductor structure.

25. A memory element as defined in claim 19, wherein said insulating layer comprises silicon dioxide.

26. A memory element as defined in claim 19, wherein said collection capacitor electrode comprises polycrystalline silicon.

27. A memory element as defined in claim 19, wherein said substrate comprises crystalline silicon.

28. A memory element as defined in claim 19, further comprising a biasing transistor having a supply input connected to receive a bias voltage, an output connected to said readout capacitor electrode, and a gate connected to receive a bias control signal, wherein, when said biasing transistor is actuated, the biasing voltage is applied to said readout capacitor electrode to thereby form a third depletion region in said substrate underneath said readout capacitor electrode with said first and third depletion regions being separated by an intervening space and said second depletion region being located within said intervening space and overlapping both said first and third depletion regions, and wherein, when said biasing transistor is not actuated, said

readout capacitor electrode is isolated from the biasing voltage to thereby enable readout of data from said readout capacitor electrode using said readout transistor.

29. A memory element as defined in claim 19, wherein said transfer electrode overlies said readout capacitor electrode and said second depletion region is located underneath said readout capacitor electrode.

30. A method of providing a non-destructive readout of analog data that is representative of the amount of incident light impinging upon a pixel element, comprising the steps of:

measuring incident light using a photocapacitor that stores charge indicative of the amount of light incident on the photocapacitor;

transferring the stored charge to a second capacitor that is not sensitive to the incident light; and

providing the charge stored on the second capacitor to an insulated gate of a transistor that is connected to supply an output signal indicative of the voltage on its insulated gate.

31. The method of claim 30, further comprising the step of gating the output signal using an output transistor.

32. The method of claim 30, further comprising the step of dumping the charge stored on the second capacitor to thereby reset the pixel element.

33. The method of claim 30, wherein said steps are carried out using silicon-based electrodes and a silicon-based substrate, and wherein said transferring step further comprises the step of transferring the stored charge between a first depletion region located in said substrate at said photocapacitor and a second depletion region located in said substrate at said second capacitor.

34. The method of claim 33, wherein said transfer step further comprises using a transfer electrode to create a third depletion region in said substrate that joins said first and second depletion regions.